



MICROCHIP

EVB-LAN9252-DIGIO
EtherCAT[®] Evaluation Board
User's Guide

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Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our website (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a “DS” number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is “DSXXXXXA”, where “XXXXX” is the document number and “A” is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the EVB-LAN9252-DIGIO. Items discussed in this chapter include:

- [Document Layout](#)
- [Conventions Used in this Guide](#)
- [The Microchip Website](#)
- [Development Systems Customer Change Notification Service](#)
- [Customer Support](#)
- [Document Revision History](#)

DOCUMENT LAYOUT

This document describes how to use the EVB-LAN9252-DIGIO as a development tool for the Microchip LAN9252 EtherCAT® slave controller. The manual layout is as follows:

- **Chapter 1. “Overview”** – This chapter shows a brief description of the EVB-LAN9252-DIGIO.
- **Chapter 2. “Board Details and Configuration”** – This chapter includes details and instructions for using the EVB-LAN9252-DIGIO.
- **Chapter 3. “LAN9252 EEPROM Programming”** – This chapter includes details and instructions for programming the LAN9252 EEPROM.
- **Appendix A. “EVB-LAN9252-DIGIO Evaluation Board”** – This appendix shows the EVB-LAN9252-DIGIO.
- **Appendix B. “EVB-LAN9252-DIGIO Evaluation Board Schematics”** – This appendix shows the EVB-LAN9252-DIGIO schematics.
- **Appendix C. “Bill of Materials (BOM)”** – This appendix includes the EVB-LAN9252-DIGIO Bill of Materials (BOM).

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	<i>MPLAB[®] IDE User's Guide</i>
	Emphasized text	...is the <i>only</i> compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	<u><i>File>Save</i></u>
Bold characters	A dialog button	Click OK
	A tab	Click the Power tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	#define START
	Filenames	autoexec.bat
	File paths	c:\mcc18\h
	Keywords	_asm, _endasm, static
	Command-line options	-Opa+, -Opa-
	Bit values	0, 1
	Constants	0xFF, 'A'
Italic Courier New	A variable argument	<i>file.o</i> , where <i>file</i> can be any valid filename
Square brackets []	Optional arguments	mcc18 [options] file [options]
Curly brackets and pipe character: { }	Choice of mutually exclusive arguments; an OR selection	errorlevel {0 1}
Ellipses...	Replaces repeated text	var_name [, var_name...]
	Represents code supplied by user	void main (void) { ... }

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- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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- **Emulators** – The latest information on Microchip in-circuit emulators. This includes the MPLAB REAL ICE and MPLAB ICE 2000 in-circuit emulators.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICkit 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are nonproduction development programmers such as PICSTART Plus and PIC-kit 2 and 3.

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- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

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Technical support is available through the website at: <http://www.microchip.com/support>

DOCUMENT REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS50002332C (10-25-19)	Chapter 2. “Board Details and Configuration”	Revised Section 2.5.1.3.1 “Fiber Mode” , Section 2.5.2 “LED Indicators” , and Section 2.5.1.3 “Copper and Fiber Straps” , and Section 2.5.1.3.2 “FX-LOS Fiber Mode Strap” . Removed Copper Mode section. Added Section 2.5.1.4 “Port Conversion from Copper to Fiber” .
	Table C-1	Added new part specifications
	All	Made minor text changes
DS50002332B (05-12-15)	All	Updated board name to “EVB-LAN9252-DIGIO” throughout document, corrected misc. typos and grammatical errors.
	Section 1.2 “References”	Updated list of application notes
DS50002332A	Initial Release of document	

NOTES:

Chapter 1. Overview

1.1 INTRODUCTION

The LAN9252 is a 2-port EtherCAT[®] slave controller with dual integrated Ethernet PHYs that each contains a full-duplex 100BASE-TX transceiver and support 100 Mbps (100BASE-TX) operation. 100BASE-FX is supported via an external fiber transceiver.

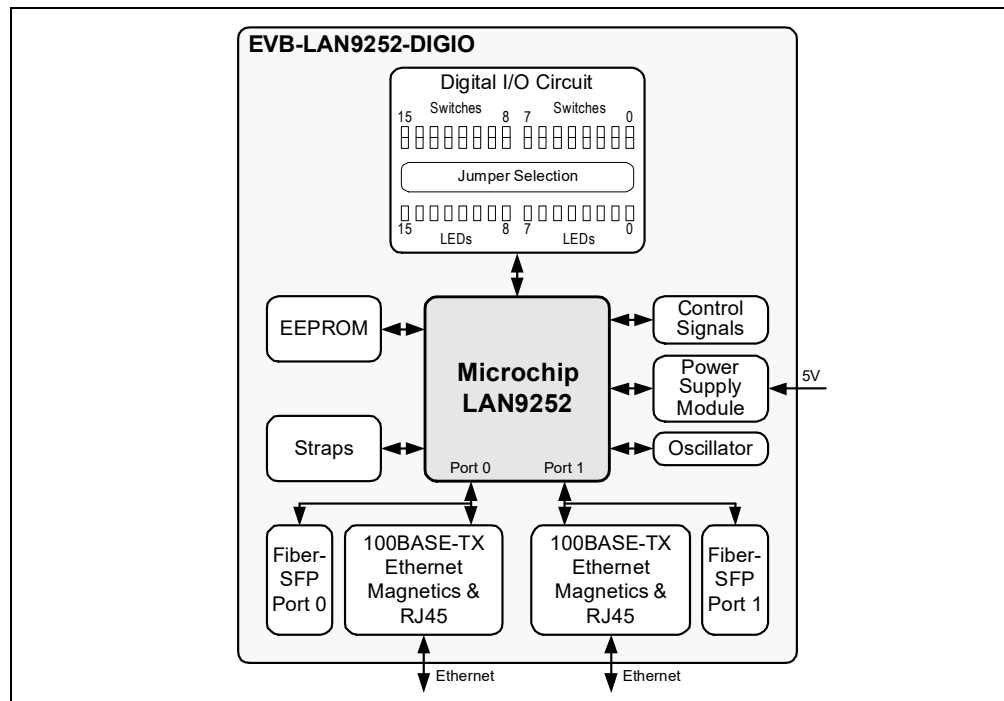
Each port receives an EtherCAT frame, performs frame checking and forwards it to the next port. Time stamps of received frames are generated when they are received. The Loop-back function of each port forwards the frames to the next logical port if there is either no link at a port, if the port is not available, or if the loop is closed for that port. The Loop-back function of port 0 forwards the frames to the EtherCAT Processing Unit. The loop settings can be controlled by the EtherCAT master.

Packets are forwarded in the order specified below. Note that Port 0 is the upstream port and must connect to an EtherCAT master, while Port 1 is the downstream port.

The EtherCAT Processing Unit (EPU) receives, analyzes, and processes the EtherCAT data stream. The main purpose of the EtherCAT Processing unit is to enable and coordinate access to the internal registers and the memory space of the ESC, which can be addressed both from the EtherCAT master and from the local application. Data exchange between master and slave applications is comparable to a dual-ported memory (process memory), enhanced by special functions for consistency checking (Sync-Manager), and data mapping (FMMU). Each FMMU performs bitwise mapping of logical EtherCAT system addresses to physical device addresses.

The scope of this document is to describe the EVB-LAN9252-DIGIO setup, which supports a Digital I/O PDI Interface and corresponding jumper configurations. The LAN9252 is connected to an RJ45 Ethernet jack with integrated magnetics for 100BASE-TX connectivity. A simplified block diagram of the EVB-LAN9252-DIGIO is shown in [Figure 1-1](#).

FIGURE 1-1: EVB-LAN9252-DIGIO BLOCK DIAGRAM



1.2 REFERENCES

Concepts and materials available in the following documents may be helpful when reading this user's guide. Visit www.microchip.com for the latest documentation.

- *LAN9252 Data Sheet*
- *AN 8.13 Suggested Magnetics*
- *EVB-LAN9252-DIGIO Schematics*
- *EVB-LAN9252-DIGIO Quick Start Guide*
- *EVB-LAN9252-HBI+ Quick Start Guide (Appendix A)*
- *AN1920 Microchip LAN9252 EEPROM Configuration and Programming Application Note*
- *AN1907 Microchip LAN9252 Migration from Beckhoff ET1100*
- *AN2007 Supporting 100BASE-FX Fiber Media for Microchip's Ethernet Controller, Switch and EtherCAT Controller Application Note*

1.3 TERMS AND ABBREVIATIONS

- DNP – Do Not Populate
- EEPROM – Electrically Erasable Programmable Read-Only Memory
- ESC – EtherCAT[®] Slave Controller
- EVB – Engineering Validation Board
- HAL – Hardware Abstraction Layer
- HBI – Host Bus Interface
- IDE – Integrated Development Environment
- LOS – Loss of Signal
- SD – Signal Detect
- SFF – Small Form Factor (fiber module, not pluggable)
- SFP – Small Form Factor Pluggable (fiber module)
- SPI – Serial Protocol Interface
- SSC – Slave Stack Code

Chapter 2. Board Details and Configuration

2.1 INTRODUCTION

This section includes subsections on the following EVB-LAN9252-DIGIO details:

- Power
- Resets
- Clock
- Configuration
- Mechanicals

2.2 POWER

2.2.1 +5V Power

Power is supplied to the LAN9252 by a +3.3V on-board regulator, which is powered by a +5V external wall adapter (Manufacturer: TRIAD MAGNETICS and P/N: WSU050-3000). The LAN9252 includes an internal +1.2V regulator which supplies power to the internal core logic. Assertion of the D1 Green LED indicates successful generation of +3.3V output. The SW1 switch must be in the ON position for the +5V to power the +3.3V regulator.

2.3 RESETS

2.3.1 Power-On Reset

A power-on reset occurs whenever power is initially applied to the LAN9252 or if the power is removed and reapplied to the LAN9252. This event resets all circuitry within the LAN9252. After initial power-on, the EVB-USB7206 Evaluation Kit can be reset by pressing the reset switch SW2. The reset LED D2 will assert (Red) if when the LAN9252 is in reset condition. For stability, a delay of approximately 180 ms is added from the +3.3V output to reset release.

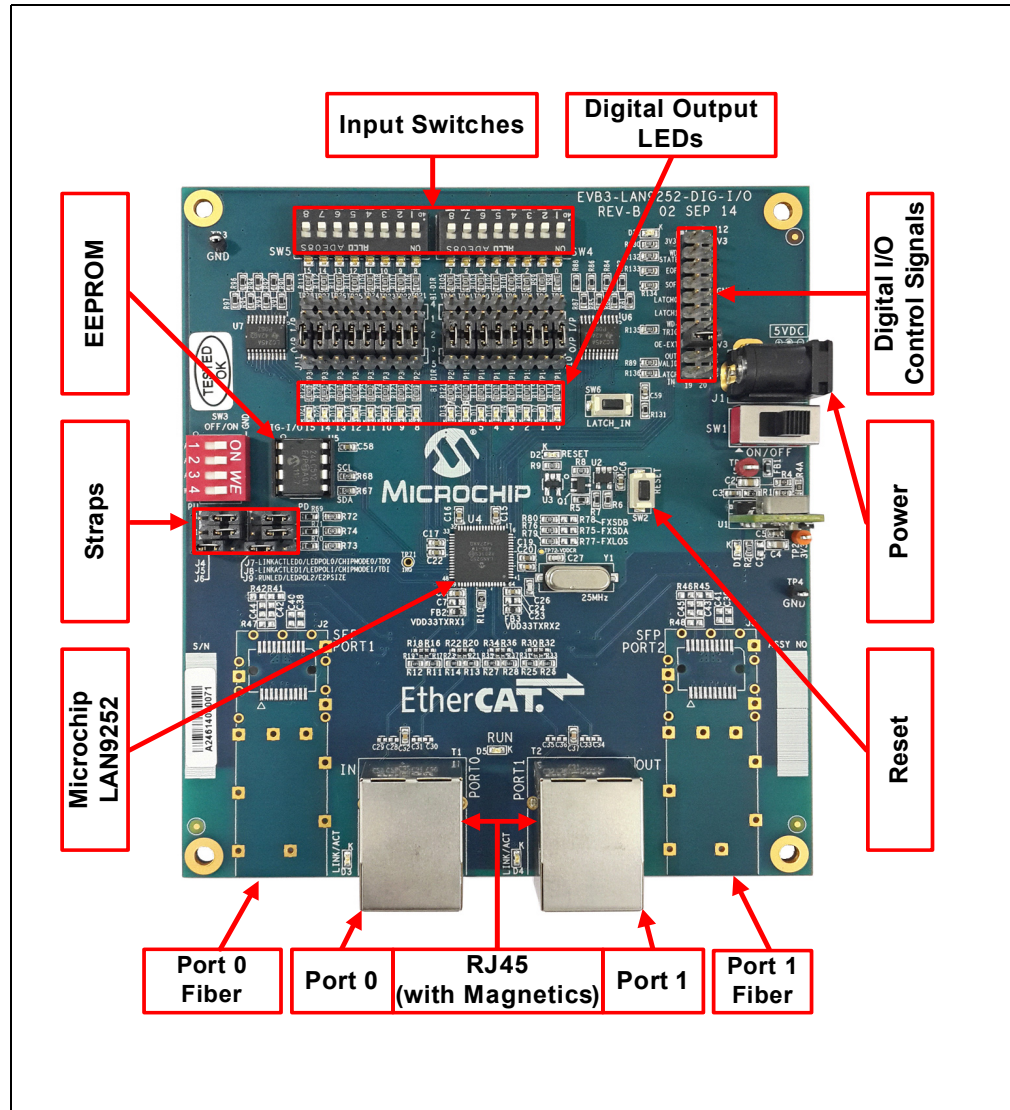
2.4 CLOCK

The EVB-LAN9252-DIGIO utilizes an external 25 MHz 25 ppm crystal from Cardinal Components Inc. (P/N: CSM1Z-A5B2C5-40-25.0D18-F).

2.5 CONFIGURATION

The following subsections describe the various board features and configuration settings. A top view of the EVB-LAN9252-DIGIO is shown in [Figure 2-1](#).

FIGURE 2-1: EVB-LAN9252-DIGIO TOP VIEW WITH CALLOUTS



2.5.1 Strap Options

2.5.1.1 CHIP MODE SELECTION

Table 2-1 details the LAN9252 Chip mode configuration straps.

TABLE 2-1: CHIP MODE CONFIGURATION STRAP

Header	Description	Pins	Settings
J4, J5, J7, J8	Chip mode configuration strap inputs. This strap determines the number of active ports and port types.	1–2 2–3	Short 1–2 for high (pull-up) (Not supported in this EVB) Short 2–3 for low (pull-down) (default)

Note: This EVB supports Chip mode 00 which is 2-port mode, where Port 0 = PHY A and Port 1 = PHY B. This requires J4, J5, J7, and J8 to be pulled-down (2–3) shorted. All other configurations are not supported by this EVB.

2.5.1.2 EEPROM SIZE CONFIGURATION

The EEPROM size configuration strap (J6 and J9) determines the supported EEPROM size range. A low selects 1 Kb (128K x 8) through 16 Kb (2K x 8)_24C16. A high selects 32 Kb (4K x 8) through 512 Kb (64K x 8) or 4 Mb (512K x 8)_24C512.

TABLE 2-2: EEPROM SIZE CONFIGURATION STRAP

Header	Description	Pins	Settings
J6, J9	EEPROM size configuration strap inputs. This strap determines the supported EEPROM size range.	1–2 2–3	Short 1–2 for high (pull-up) (default) Short 2–3 for low (pull-down)

2.5.1.3 COPPER AND FIBER STRAPS

The LAN9252 supports 100BASE-TX (Copper) and 100BASE-FX (Fiber) modes. In 100BASE-FX operation, the presence of the receive signal is indicated by the external transceiver as either an open-drain, CMOS level, Loss of Signal (SFP) or a LVPECL Signal Detect (SFF).

This EVB supports 100BASE-TX (Copper) and SFP 100BASE-FX (Fiber) modes. By default, Copper mode is active. Fiber mode is supported as an assembly option. To select the Copper or Fiber mode, the respective strap and signal routing resistor assembly options must be configured.

2.5.1.3.1 Fiber Mode

The EVB-LAN9252-DIGIO board uses SFP modules to implement the fiber interface. The LAN9252 can be configured to work with either signal detect (SD) or loss of signal (LOS) signaling from the fiber module. All SFP modules use LOS. In LOS mode, the LAN9252 can be strapped for any of three configurations:

- Configuration 1: Port 0 copper, Port 1 copper (See Table 2-3.)
- Configuration 2: Port 0 fiber, Port 1 copper (See Table 2-4.)
- Configuration 3: Port 0 fiber, Port 1 fiber (See Table 2-5.)

The fourth configuration—Port 0 copper, Port 1 fiber—is invalid in fiber LOS mode.

TABLE 2-3: STRAPPING FOR CONFIGURATION 1

Resistors	Description
R77	DNP
R79	10 kΩ
R75	DNP
R76	10 kΩ
R78	DNP
R80	10 kΩ

TABLE 2-4: STRAPPING FOR CONFIGURATION 2

Resistors	Description
R77	10 kΩ
R79	10 kΩ
R75	10 kΩ
R76	DNP
R78	DNP
R80	10 kΩ

TABLE 2-5: STRAPPING FOR CONFIGURATION 3

Resistors	Description
R77	10 kΩ
R79	DNP
R75	10 kΩ
R76	DNP
R78	10 kΩ
R80	DNP

2.5.1.3.2 FX-LOS Fiber Mode Strap

FX-LOS strap details are shown in [Table 2-6](#). These strap settings determine if the ports are to operate in Fiber mode or Copper mode.

TABLE 2-6: FX-LOS MODE STRAP SETTINGS

R77 (10K)	R79 (10K)	Reference Voltage (V)	Function
Populate	DNP	3.3	A level above 2V selects Fiber mode for Port 0 and Port 1.
Populate	Populate	1.5	A level greater than 1V and below 2V selects Fiber mode for Port 0 and Copper mode for Port 1.
DNP	Populate	0 (Default)	A level of 0V selects Copper mode for Ports 0 and 1.

2.5.1.4 PORT CONVERSION FROM COPPER TO FIBER

To convert a port from copper to fiber, install or move the components specified in the following [Table 2-7](#) and [Table 2-8](#).

The surface mount SFP receptacle is part number 1367073-1 from TE Connectivity. The press-fit SFP cage is part number U77-A1118-200T from Amphenol. Examples of the SFP module are part number LM38-A3S-TI-N from ATOP Technologies, or FTLF1217P2 from Finisar.

TABLE 2-7: PORT 0 MODIFICATIONS FOR FIBER

J2	SFP receptacle and SFP cage
Move 0Ω from R17, R19, R21, R23 to R16, R18, R20, R22	
R41, R42	49.9 kΩ
C38, C40, C42, C44	0Ω
R47	DNP
C48, C54	10 μF
C47, C49, C55	0.1 μF
C46	DNP
L2, L4	1 μH
R53, R54, R55, R56	4.7 kΩ
R39, R40	82Ω
R49, R50	130Ω

TABLE 2-8: PORT 1 MODIFICATIONS FOR FIBER

J3	SFP receptacle and SFP cage
Move 0Ω from R31, R33, R35, R37 to R30, R32, R34, R36	
R45, R46	49.9 kΩ
C39, C41, C43, C45	0Ω
R48	DNP
C52, C56	10 μF
C51, C53, C57	0.1 μF
C50	DNP
L1, L3	1 μH
R57, R58, R59, R60	4.7 kΩ
R43, R44	82Ω
R51, R52	130Ω

2.5.2 LED Indicators

The D3 and D4 LEDs are used to indicate the Link/Activity status on the corresponding EVB ports, as detailed in [Table 2-9](#). The Link/Act LED should be ON at each port when the cable is present. If the Link/Act LED is not ON, it indicates there is an issue with the connection or cable.

TABLE 2-9: D3 AND D4 LINK/ACTIVITY LED STATUS INDICATORS

State	Description
Off	Link is down.
Flashing Green	Link is up with activity.
Steady Green	Link is up with no activity.

Additionally, the D5 LED is used as a RUN indicator (green) to show the AL status of the EtherCAT[®] State Machine (ESM), as detailed in [Table 2-10](#).

TABLE 2-10: D5 RUN LED STATUS INDICATOR

State	Description
Off	The device is in the INITIALIZATION state.
Blinking (on 200 ms, off 200 ms)	The device is in the PRE-OPERATIONAL state.
Single Flash (on 200 ms, off 1000 ms)	The device is in the SAFE-OPERATIONAL state.
On	The device is in the OPERATIONAL state.
Flickering (on 50 ms, off 50 ms)	The device is booting and has not yet entered the INITIALIZATION state, or the device is in the BOOTSTRAP state and firmware download is in progress. (Optional. Off when not implemented.)

2.5.3 EEPROM Switch

The EVB-LAN9252-DIGIO utilizes 0x50 (7-bit) I²C slave addressing. The SW3 switch can be used to select the A0, A1, and A2 address bits, as shown in [Figure 2-2](#) and [Table 2-11](#). The eighth bit of the slave address determines if the master device wants to read or write to the EEPROM (24C512).

FIGURE 2-2: SLAVE ADDRESS ALLOCATION

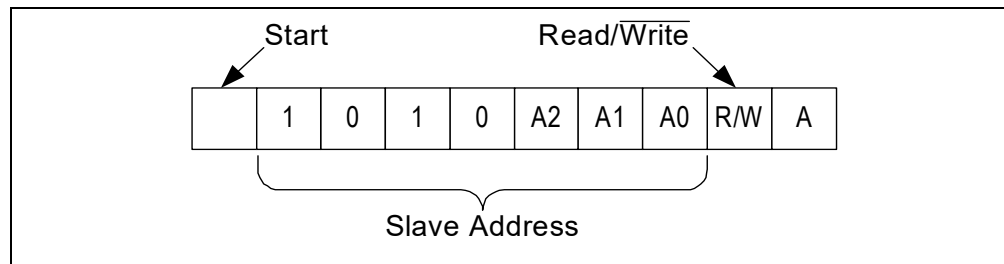


TABLE 2-11: EEPROM SWITCH

Switch	Description	Settings
SW3	I ² C EEPROM address selection switch (A0, A1, A2). See Figure 2-2 .	ON for logic 0 (default) OFF for logic 1

2.5.4 DIG INPUT Mode

The DIG INPUT mode can be selected through the headers J10 and J11:

- Logic 1: (Default) SW4 and SW5 Off position. DIG I/P 0 to 15 tied to pull-up (R98 to R113)
- Logic 0: The respective knobs of 2-way, 8-position dip switch (SW4 and SW5) need to be moved to ON position. Signals can be selected individually.

TABLE 2-12: DIGITAL I/O INPUT MODE SELECTION

Header	Description	Short Pins
J10	Digital Input 0 to 7	1&2, 4&5, 7&8, 10&11, 13&14, 16&17, 19&20, 22&23
J11	Digital Input 8 to 15	1&2, 4&5, 7&8, 10&11, 13&14, 16&17, 19&20, 22&23

2.5.5 DIG OUTPUT Mode

The DIG OUTPUT Mode can be selected through the headers J10 and J11. The updated Digital I/O values can be seen on the LEDs (D6 to D21):

- Logic 1: LED illuminated
- Logic 0: LED not illuminated.

Note: LED (D6 to D21) anode connected to ASIC.

TABLE 2-13: DIGITAL I/O OUTPUT MODE SELECTION (DEFAULT MODE)

Header	Description	Short Pins
J10	Digital I/O 0 to 7	2&3, 5&6, 8&9, 11&12, 14&15, 17&18, 20&21, 23&24
J11	Digital I/O 8 to 15	2&3, 5&6, 8&9, 11&12, 14&15, 17&18, 20&21, 23&24

Note: The control signal OE_EXT should be connected high by shorting J12 pins 15 and 16.

2.5.6 DIG Bidirectional Mode

The DIG Bidirectional mode can be selected by shorting the respective test point pins with the headers J10 and J11, as detailed in [Table 2-14](#). The input and output signal states in this mode are the same as detailed in [Section 2.5.4 “DIG INPUT Mode”](#) and [Section 2.5.5 “DIG OUTPUT Mode”](#).

TABLE 2-14: DIGITAL I/O BIDIRECTIONAL MODE DESCRIPTION

Description	Short Pins
Digital I/O 0 to 7	TP5 & J10.1, TP6 & J10.4, TP7 & J10.7, TP8 & J10.10 TP9 & J10.13, TP10 & J10.16, TP11 & J10.19, TP12 & J10.22, TP13&J10.3, TP14&J10.6, TP15&J10.9, TP16& J10.12, TP17&J10.15, TP18&J10.18, TP19& J10.21, TP20&J10.24
Digital I/O 8 to 15	TP21 & J11.1, TP22 & J11.4, TP23 & J11.7, TP24 & J11.10, TP25 & J11.13, TP26 & J11.16, TP27 & J11.19, TP28 & J11.22, TP29&J11.3, TP30&J11.6, TP31&J11.9, TP32& J11.12, TP33&J11.15, TP34&J11.18,TP35& J11.21, TP36&J11.24

2.5.7 Control Signals

All control signals can be probed and controlled via the J12 header, as shown in [Table 2-15](#).

TABLE 2-15: J12 HEADER CONTROL SIGNAL MAPPING

J12 Pin Number	J12 Signal	J12 Pin Number	J12 Signal
1	3V3	2	3V3
3	WD_STATE	4	GND
5	EOF	6	GND
7	SOF	8	GND
9	LATCH0	10	GND
11	LATCH1	12	GND

TABLE 2-15: J12 HEADER CONTROL SIGNAL MAPPING (CONTINUED)

J12 Pin Number	J12 Signal	J12 Pin Number	J12 Signal
13	WD_TRIG	14	GND
15	OE_EXIT	16	3V3
17	OUTVALID	18	GND
19	LATCH_IN	20	GND

Note: J12 pins 15 and 16 must be shorted in Output mode.

2.5.7.1 WD_STATE

This pin is the SyncManager Watchdog State output. A “0” indicates the watchdog has expired. The state of this signal can be seen in the LED D22.

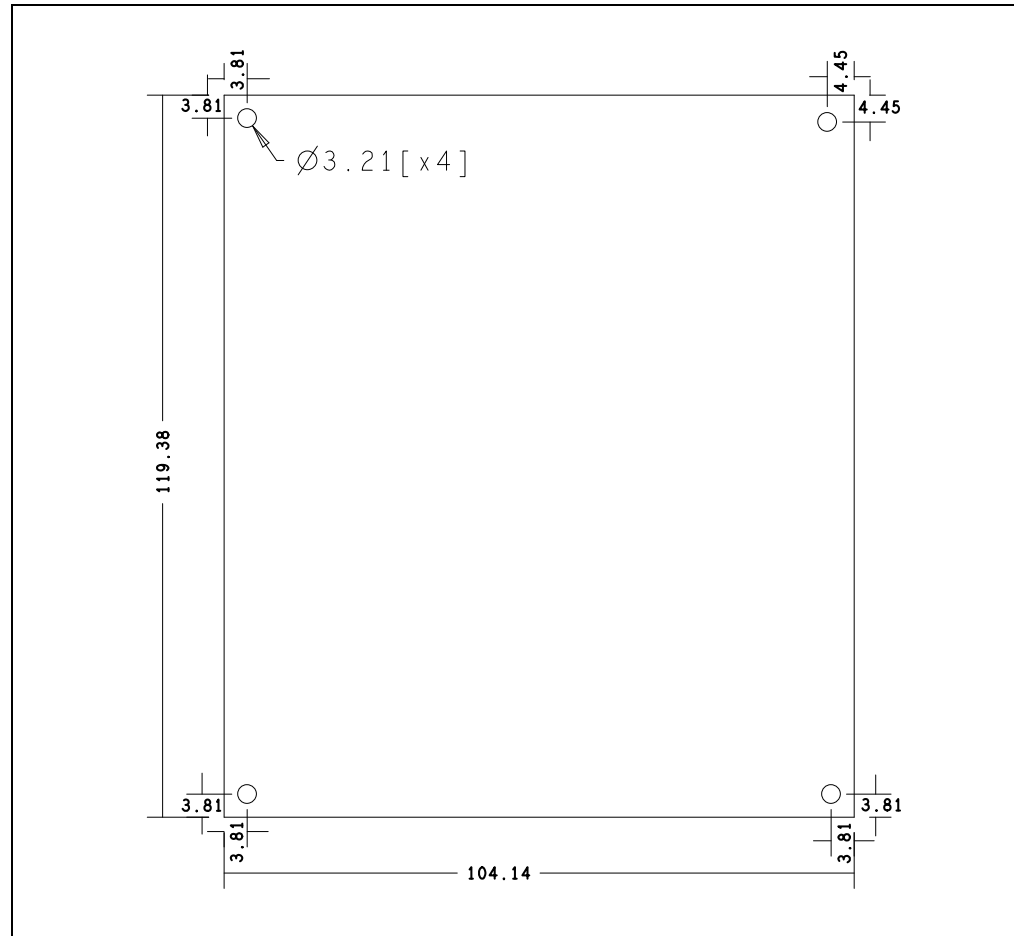
Note: This signal is not driven (high impedance) until the EEPROM is loaded.

2.5.7.2 LATCH_IN

This pin is the external data latch signal. The input data is sampled each time a rising edge of LATCH_IN is recognized. By default, this signals is pulled high through R131 and can be made low using switch SW6.

2.6 MECHANICALS

FIGURE 2-3: EVB-LAN9252-DIGIO MECHANICAL DIMENSIONS



Chapter 3. LAN9252 EEPROM Programming

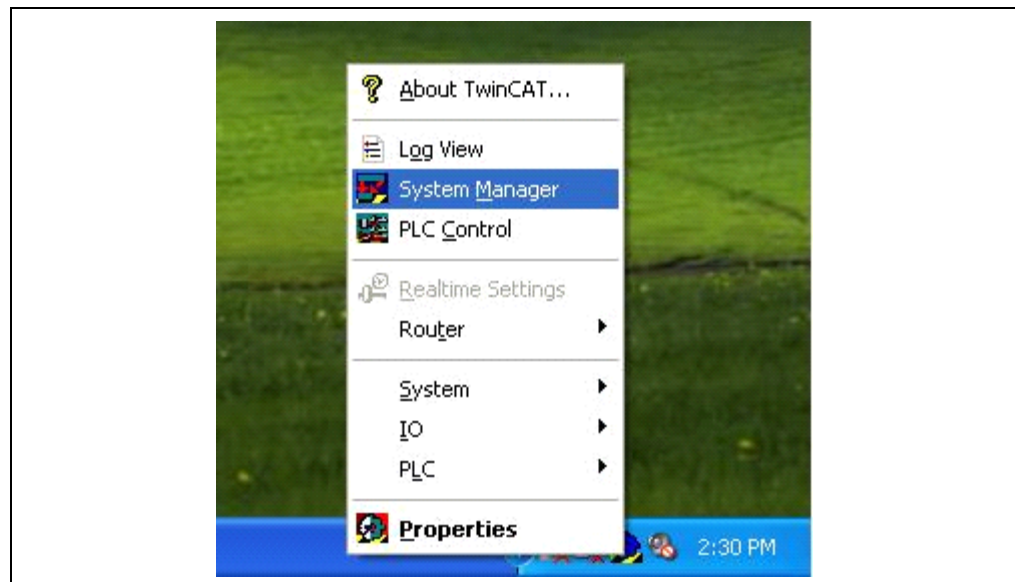
3.1 PROGRAMMING THE LAN9252 EEPROM

The LAN9252 configures itself to the desired mode (SPI, 6 HBI modes) by reading the strap settings located in EEPROM. The LAN9252 EEPROM is programmed and validated via the TwinCAT master tool. The programming procedure is as follows:

1. Load the corresponding ESI file in the directory path C:\TwinCAT\Io\EtherCAT. For this demo, the ESI file for the 16-Bit Multiplexed Single-Phase mode is used.
2. If TwinCAT installed successfully, a TwinCAT icon will be shown in the bottom-right corner of the desktop. After clicking the icon, a pop-up list will display. Select System Manager, as shown in [Figure 3-1](#).

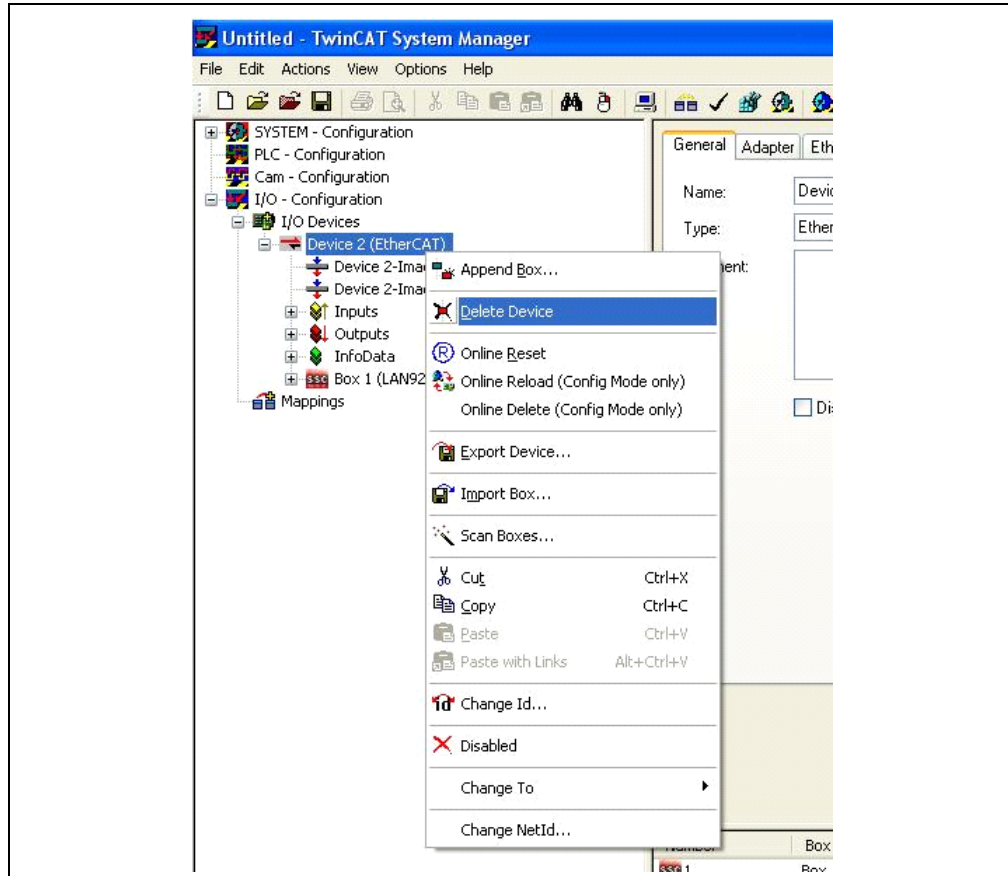
- Note 1:** This example utilizes the TwinCAT tool. Procedures may differ when using other EtherCAT® master tools.
- 2: For more information on TwinCAT EtherCAT master installation, please refer to the *EVB-LAN9252-DIGIO Quick Start Guide*. The document is found in the Board Support Package for EVB-LAN9252-DIGIO on the Microchip website.
 - 3: Ensure the system network properties are configured properly for the EtherCAT frames, Ethernet cable linking your system, and EtherCAT slave board.

FIGURE 3-1: TWINCAT SYSTEM MANAGER



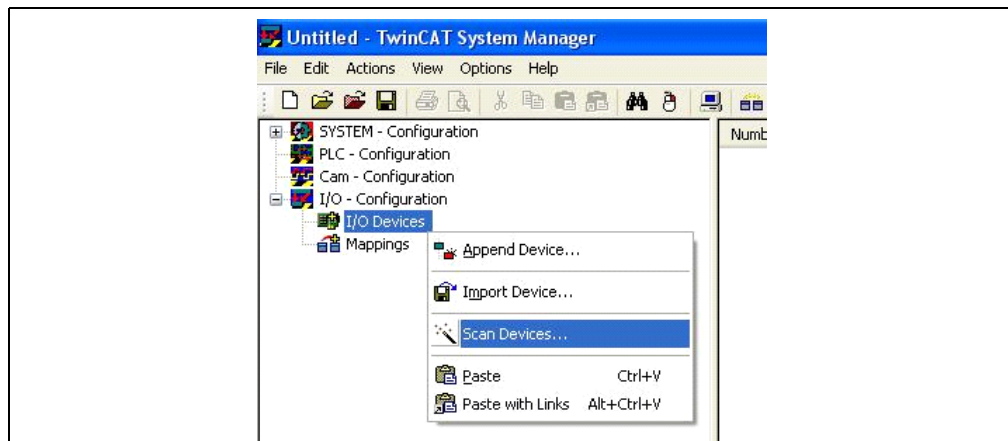
3. If any devices are present, delete them accordingly by clicking the device and selecting Delete Device, as shown in [Figure 3-2](#).

FIGURE 3-2: TWINCAT DELETE DEVICE



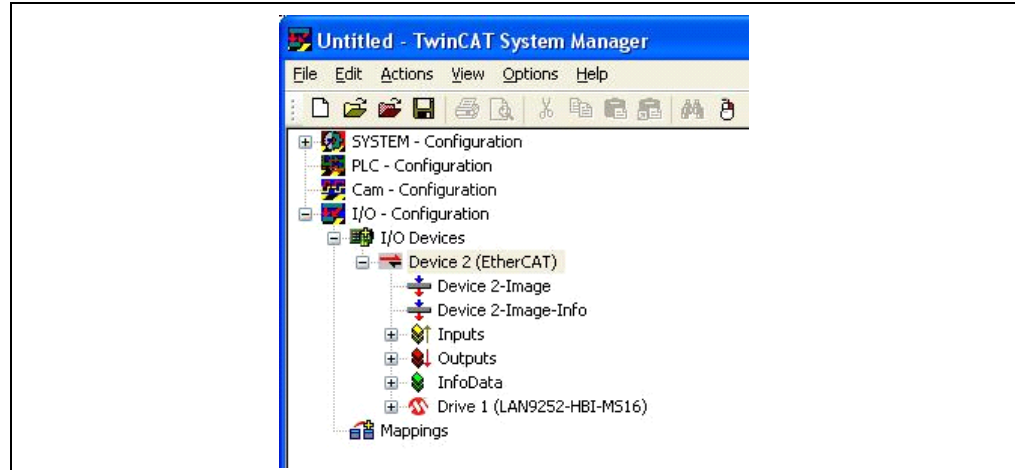
4. Scan for EtherCAT slave devices by clicking I/O devices and selecting Scan Devices, as shown in [Figure 3-3](#).

FIGURE 3-3: TWINCAT SCAN DEVICES



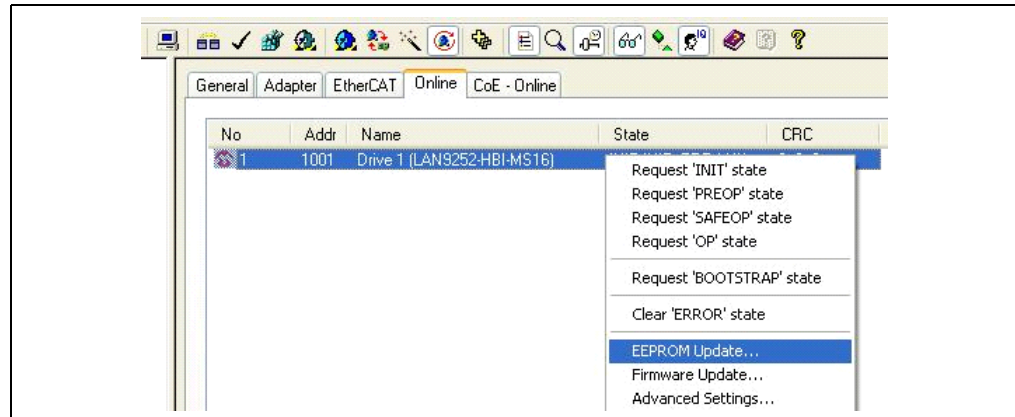
5. After scanning is complete, the right panel of the TwinCAT window appears as shown in [Figure 3-4](#).

FIGURE 3-4: TWINCAT DEVICE LIST



6. After a successful scan, click the Device 2 (EtherCAT) dropdown bar on the left panel of the TwinCAT tool (as highlighted in [Figure 3-4](#)). Then click the **Online** tab on the right-side panel of the TwinCAT tool, as shown in [Figure 3-5](#). Right click the LAN9252 listing and select EEPROM Update from the contextual menu.

FIGURE 3-5: TWINCAT EEPROM UPDATE



7. Upon selecting EEPROM Update, the Write EEPROM window will open. Click the **OK** button to initiate EEPROM programming.

FIGURE 3-6: TWINCAT WRITE EEPROM

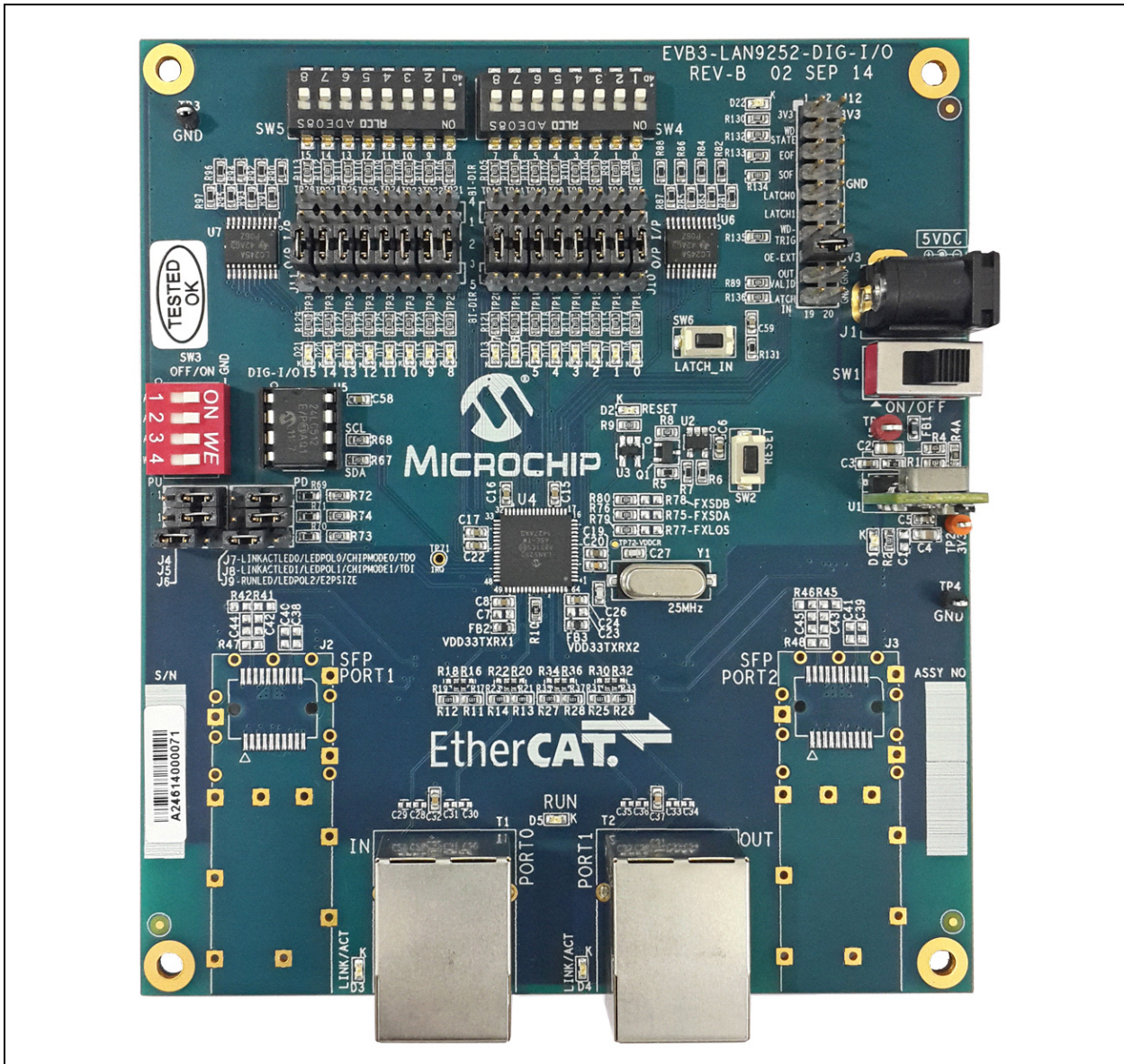


NOTES:

Appendix A. EVB-LAN9252-DIGIO Evaluation Board

This appendix shows the EVB-LAN9252-DIGIO Evaluation Kit Evaluation Board.

FIGURE A-1: EVB-LAN9252-DIGIO EVALUATION KIT EVALUATION BOARD



NOTES:



Appendix B. EVB-LAN9252-DIGIO Evaluation Board Schematics

B.1 INTRODUCTION

This appendix shows the EVB-LAN9252-DIGIO Evaluation Board Schematics.

FIGURE B-2: EVB-LAN9252-DIGIO SCHEMATIC LAN9252 PT1

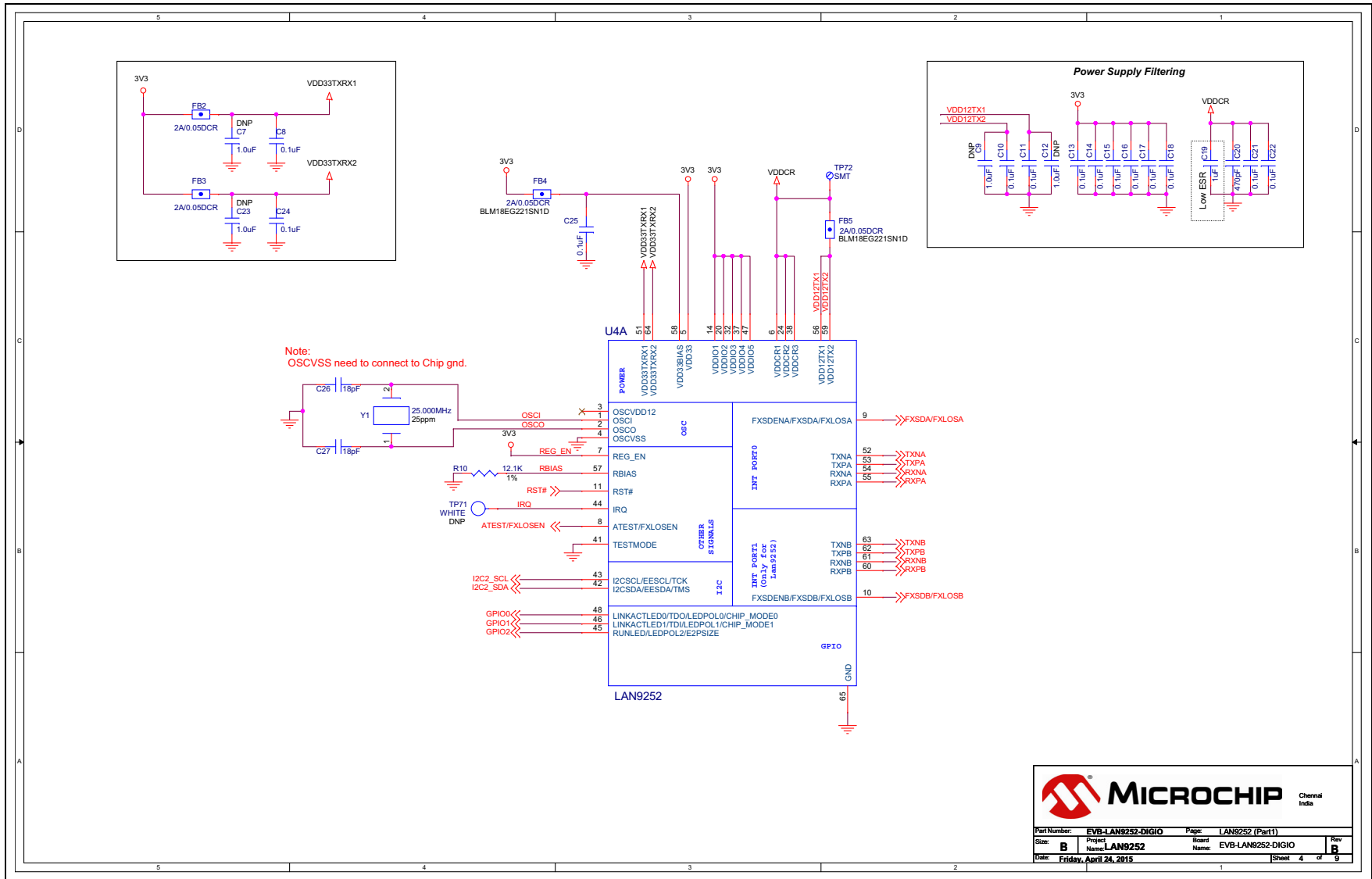
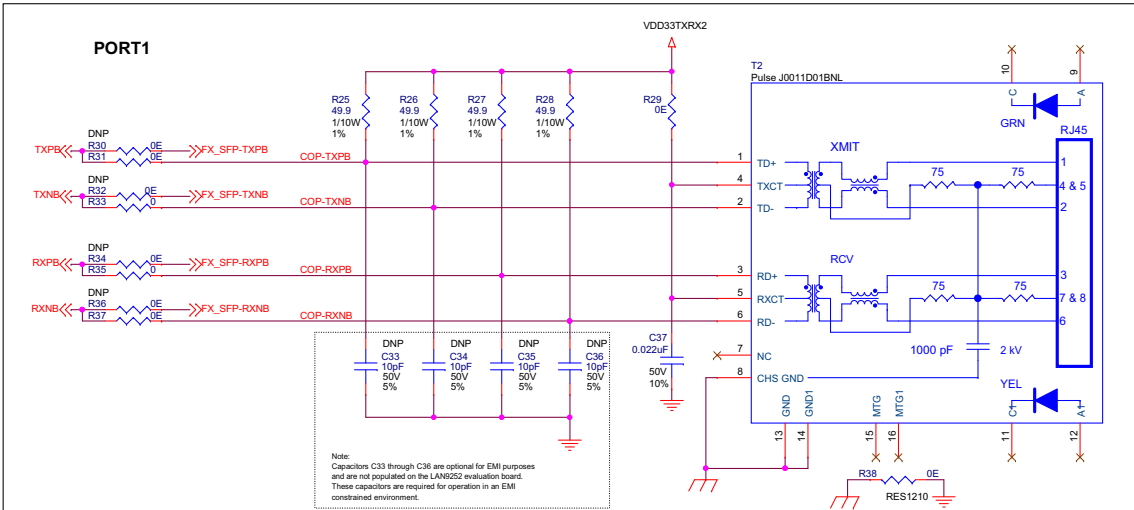
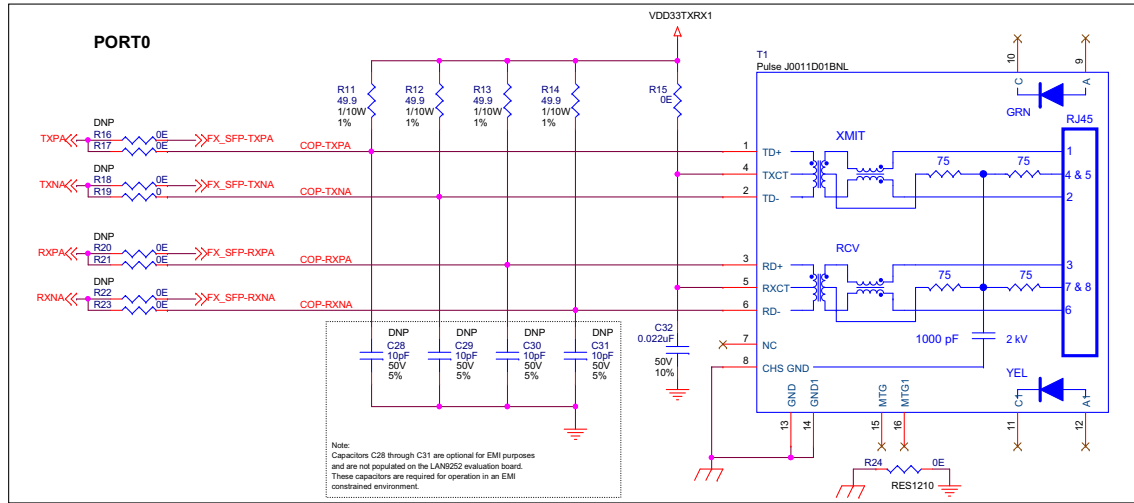


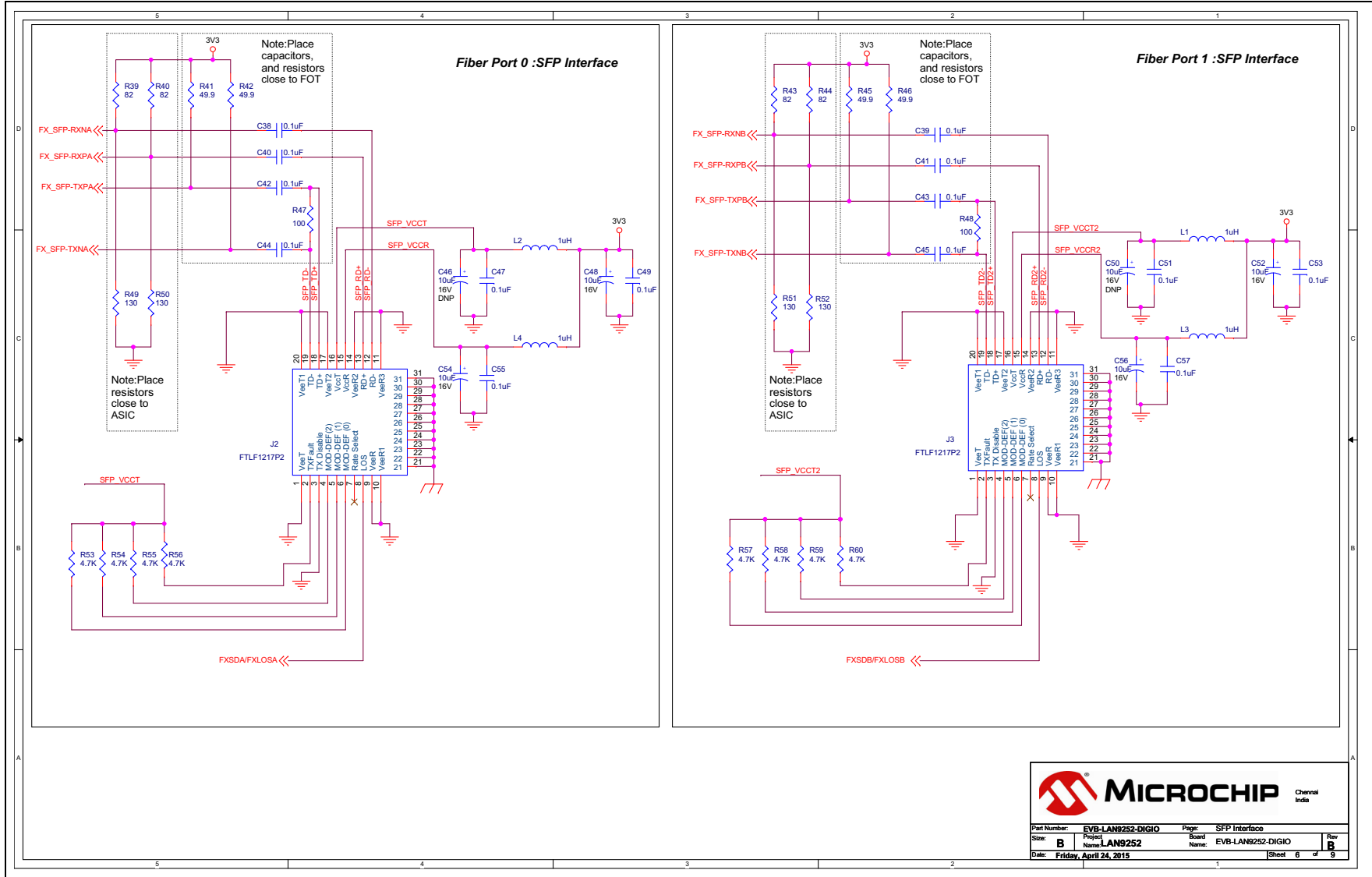
FIGURE B-3: EVB-LAN9252-DIGIO SCHEMATIC COPPER MODE INTERFACE



MICROCHIP Channel India

Part Number:	EVB-LAN9252-DIGIO	Page:	Copper Mode Interface
Size:	B	Project Name:	LAN9252
Date:	Friday, April 24, 2015	Board Name:	EVB-LAN9252-DIGIO
		Rev:	B
		Sheet:	5 of 9

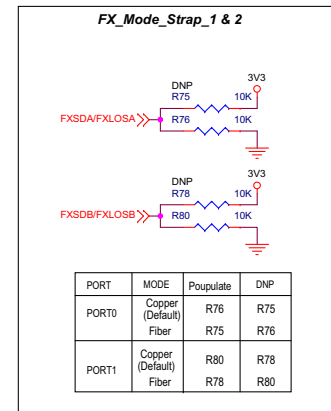
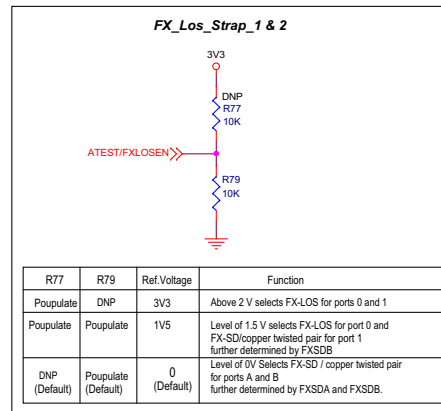
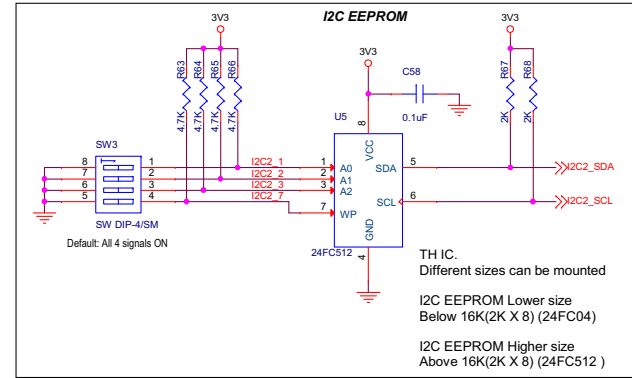
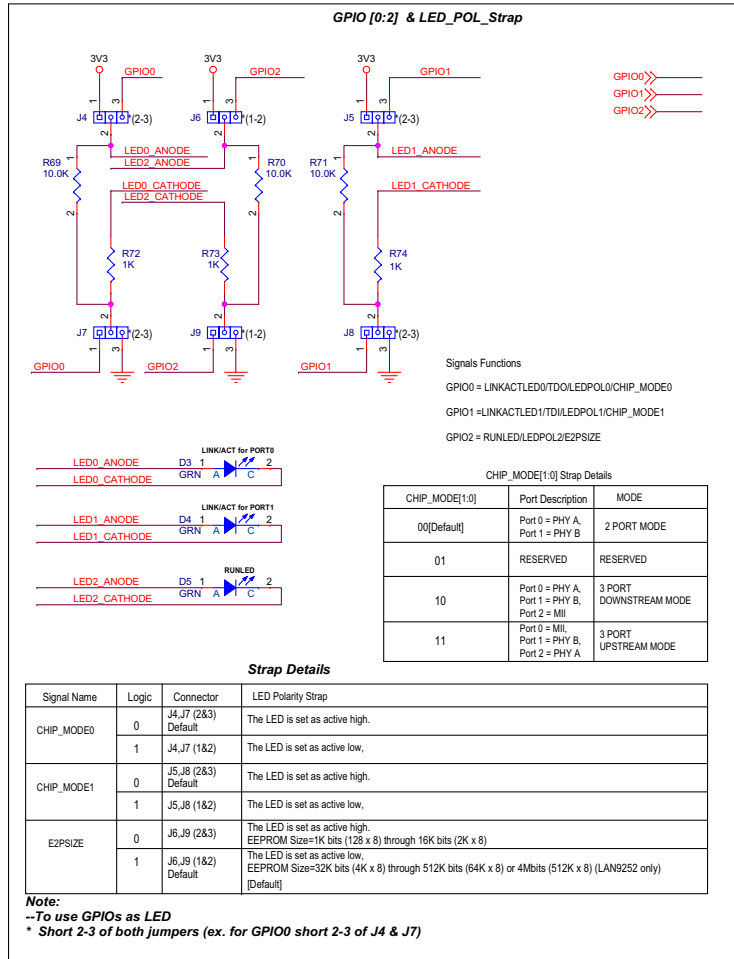
FIGURE B-4: EVB-LAN9252-DIGIO SCHEMATIC SFP INTERFACE



MICROCHIP Channel Inds

Part Number:	EVB-LAN9252-DIGIO	Page:	SFP Interface
Size:	B	Project Name:	LAN9252
Date:	Friday, April 24, 2015	Board Name:	EVB-LAN9252-DIGIO
		Rev:	1
		Sheet:	6 of 9

FIGURE B-5: EVB-LAN9252-DIGIO SCHEMATIC STRAP, GPIO, I2C & FXLOS



MICROCHIP Channel India

Part Number:	EVB-LAN9252-DIGIO	Page:	STRAP,GPIO,I2C & FXLOS
Size:	B	Project Name:	EVB-LAN9252-DIGIO
Date:	Friday, April 24, 2015	Sheet:	7 of 9

FIGURE B-6: EVB-LAN9252-DIGIO SCHEMATIC LAN9252 PT2

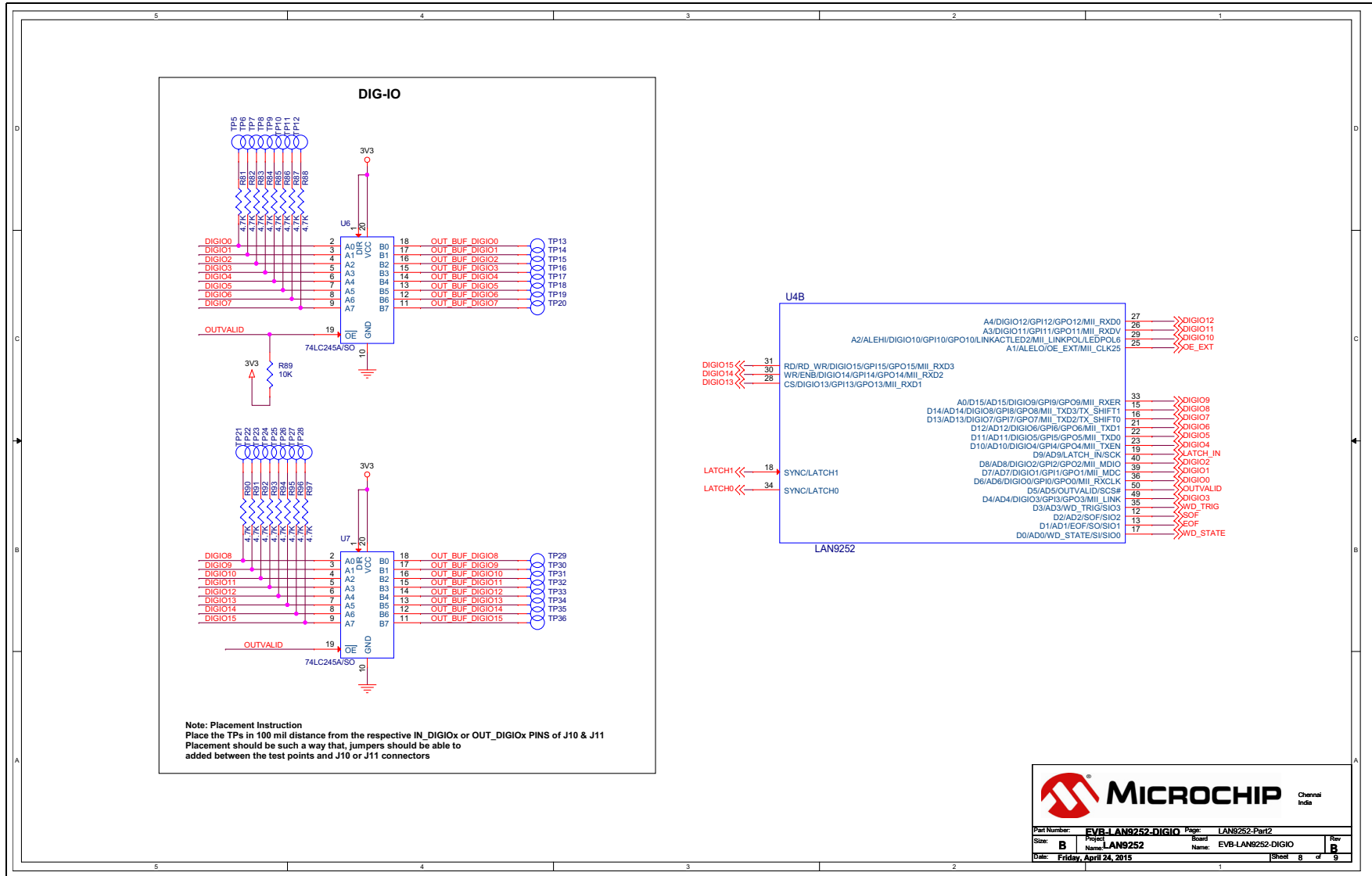
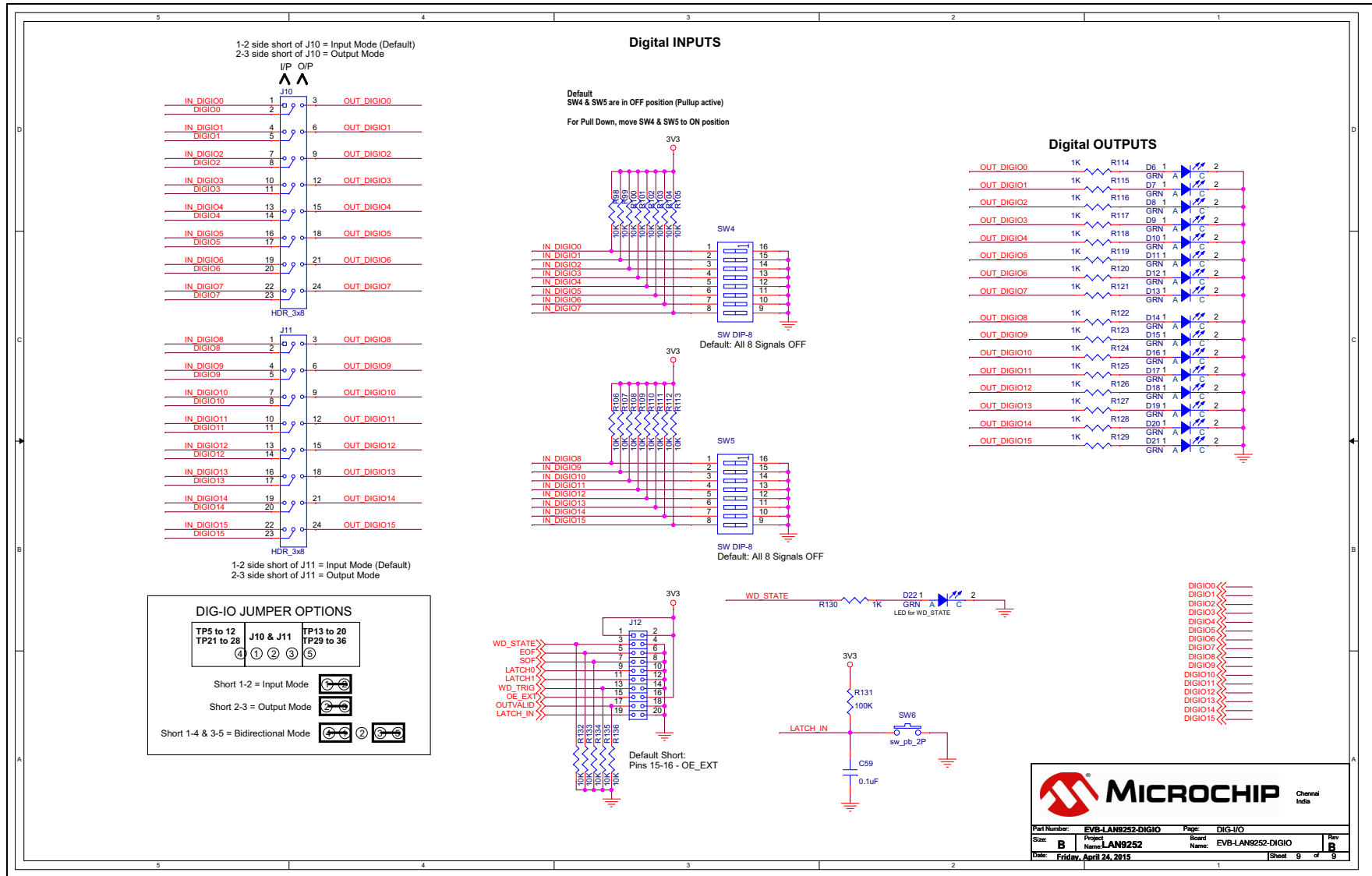


FIGURE B-7: EVB-LAN9252-DIGIO SCHEMATIC DIGITAL I/O



MICROCHIP Channel India

Part Number:	EVB-LAN9252-DIGIO	Page:	DIG-I/O
Size:	B	Project Name:	LAN9252
Date:	Friday, April 24, 2015	Board Name:	EVB-LAN9252-DIGIO
		Sheet:	9 of 9



Appendix C. Bill of Materials (BOM)

C.1 INTRODUCTION

This appendix includes the EVB-LAN9252-DIGIO Evaluation Board Bill of Materials (BOM).

TABLE C-1: BILL OF MATERIALS

Item	Quantity	Reference	Part	PCB Footprint	DNP	Vendor	Vendor Part NO
1	2	C2,C4	10uF	CAP0805	No	Murata	GRM21BR61E106KA73L
2	18	C3,C5,C6,C8,C10,C11,C13,C14,C15,C16,C17,C18,C21,C22,C24,C25,C58,C59	0.1uF	CAP0603	No	Murata	GRM188R71E104KA01D
3	1	C19	1uF	CAP0603	No	Murata	GRM188R61C105KA93D
4	1	C20	470pF	CAP0603	No	Kemet	C0603C471K3RACTU
5	2	C26,C27	18pF	CAP0603	No	Murata	GRM1885C1H180JA01D
6	2	C32,C37	0.022uF	CAP0603	No	Kemet	C0603C223K5RACTU
7	21	D1,D3,D4,D5,D6,D7,D8,D9,D10,D11,D12,D13,D14,D15,D16,D17,D18,D19,D20,D21,D22	GRN	LED0603	No	Wurth electronics	150 060 GS7 500 0
8	1	D2	RED	LED0603	No	Wurth electronics	150 060 RS7 500 0
9	5	FB1,FB2,FB3,FB4,FB5	2A/0.05DCR	RES0603	No	Murata	BLM18EG221SN1D
10	1	J1	SKT_PWR_2R0mm_4A_THRU_RA	th_conn_pwrjack_dc-210_rt	No	Cui Stack	PJ-002AH
11	6	J4,J5,J6,J7,J8,J9	HDR_1x3	TH_CONN_1X3P	No	FCI	68000-103HLF
12	2	J10,J11	HDR_3x8	TH_CONN_3x8P	No	FCI	68000-108HLF
13	1	J12	2x10	TH_CONN_2x10P	No	FCI	67997-220HLF
14	1	Q1	NDS355AN_NMOS	sot23-NDS	No	Fairchild	NDS355AN
15	3	R1,R15,R29	0E	RES0603	No	Panasonic	ERJ-3GEY0R00V
16	22	R2,R8,R72,R73,R74,R114,R115,R116,R117,R118,R119,R120,R121,R122,R123,R124,R125,R126,R127,R128,R129,R130	1K	RES0603	No	Panasonic	ERJ-3GEYJ102V
17	1	R3	3.30K	RES0603	No	Yageo America	9C06031A3301FKHFT
18	1	R4	470E	RES0603	No	BOURNS	CR0603-FX-4700ELF
19	1	R4A	33E	RES0603	No	BOURNS	CR0603-FX-33R0ELF
20	1	R5	4.75K	RES0603	No	Panasonic	ERJ-3EKF4751V
21	4	R6,R69,R70,R71	10.0K	RES0603	No	Panasonic	ERJ-3EKF1002V
22	1	R7	100	RES0603	No	Panasonic	ERJ-3EKF1000V
23	1	R9	2.2K	RES0603	No	Panasonic	ERJ-3GEYJ222V
24	1	R10	12.1K	RES0603	No	Rohm	MCR01MZPF1202
25	8	R11,R12,R13,R14,R25,R26,R27,R28	49.9	RES0603	No	Yageo America	9C06031A49R9FKHFT
26	8	R17,R19,R21,R23,R31,R33,R35,R37	0E	RES0402	No	Panasonic	ERJ-2GE0R00X

27	2	R24,R38	0E	RES1210	No	Vishay	CRCW12100000Z0EA
28	2	R67,R68	2K	RES0603	No	Panasonic	ERJ-3GEYJ202V
29	25	R76,R79,R80,R89,R98,R99,R100,R101,R102,R103,R104,R105,R106,R107,R108,R109,R110,R111,R112,R113,R132,R133,R134,R135,R136	10K	RES0603	No	Panasonic	ERJ-3GEYJ103V
30	1	R131	100K	RES0603	No	Panasonic	ERJ-3EKF1003V
31	20	R81,R82,R83,R84,R85,R86,R87,R88,R90,R91,R92,R93,R94,R95,R96,R97,R63,R64,R65,R66	4.7K	RES0603	No	Panasonic	ERJ-3EKF4701V
32	1	SW1	SW-SPDT-SLIDE	sw_ck_1101m2s3cq2	No	C&K	1101M2S3CQE2
33	2	SW2,SW6	sw_pb_2P	sw_pb_2P	No	Panasonic	EVQ-PJU04K
34	1	SW3	SW DIP-4/SM	TH_SW_DIP4	No	Würth electronics	418117270904
35	2	SW4,SW5	SW DIP-8	SW_DIP_SMT_8P-ade08s04	No	TE	1-1825058-9/ade08s04
36	1	TP1	RED	TH_TP_60D40	No	Keystone	5000
37	1	TP2	ORANGE	TH_TP_60D40	No	Keystone	5003
38	2	TP3,TP4	BLACK	TH_TP_60D40	No	Keystone	5001
39	32	TP5,TP6,TP7,TP8,TP9,TP10,TP11,TP12,TP13,TP14,TP15,TP16,TP17,TP18,TP19,TP20,TP21,TP22,TP23,TP24,TP25,TP26,TP27,TP28,TP29,TP30,	WHITE	TH_TP	No	FCI	68000-101HLF
40	2	T1,T2	Pulse - J0011D01BNL	th_conn_pulse_rj45_j0026	No	Pulse Electronics	J0011D01BNL
41	1	U1	3_Amp	TH_DC-DC_VERT_5PIN_P67	No	Murata	OKR-T/3-W12-C
42	1	U2	TPS3125	SOT23_5	No	TI	TPS3125L30DBVR
43	1	U3	74LVC1G14	SOT23_5	No	TI	SN74LVC1G14DBVR
44	1	U4	LAN9252	IC_QFN64	No	Microchip	LAN9252
45	1	U5	24FC512	IC_DIP8_300	No	Microchip	24FC512-I/P
46	2	U6,U7	74LC245A/SO	IC_SO20-MO-153	No	TI	SN74LVC245APWR
47	1	Y1	25.000MHz	XTAL_HCM49	No	Cardinal Components Inc.	CSM1Z-A5B2C5-40-25.0D18-F

Do NOT Populate components:							
Item	Quantity	Reference	Part	PCB Footprint	DNP	Vendor	Vendor Part NO
1	1	C1	4.7uF	CAP0603	DNP	Murata	GRM188R60J475KE19D
2	4	C7,C9,C12,C23	1.0uF	CAP0603	DNP	Murata	GRM188R61C105KA93D
3	8	C28,C29,C30,C31,C33,C34,C35,C36	10pF	CAP0402	DNP	Murata	GRM1885C1H100JA01D
4	14	C38,C39,C40,C41,C42,C43,C44,C45,C47,C49, C51,C53,C55,C57	0.1uF	CAP0603	DNP	Murata	GRM188R71E104KA01D
5	6	C46,C48,C50,C52,C54,C56	10uF	CAP_B_3528	DNP	Kemet	B45190E3106K209
6	2	J2,J3	FTLF1217P2	CONN_FX_SFP_FTLF1217P2	DNP	Finisar	775-1011-ND
7	2	J2, J3	SMT SFP receptacle	-	DNP	TE Connectivity	1367073-1
8	2	J2, J3	SFP press-fit cage	SFP	DNP	Amphenol	U77A1118-200T
9	4	L1,L2,L3,L4	1uH	L0805	DNP		
10	8	R16,R18,R20,R22,R30,R32,R34,R36	0	RES0402	DNP		
11	4	R39,R40,R43,R44	82	RES0603	DNP	Panasonic	ERJ-3EKF1300V
12	4	R41,R42,R45,R46	49.9	RES0603	DNP	Yageo America	9C06031A49R9FKHFT
13	2	R47,R48	100	RES0603	DNP	Panasonic	ERJ-3EKF1000V
14	4	R49,R50,R51,R52	130	RES0603	DNP	Panasonic	ERJ-3EKF1300V
15	8	R53,R54,R55,R56,R57,R58,R59,R60	4.7K	RES0603	DNP	Panasonic	ERJ-3EKF4701V
16	3	R75,R77,R78	10K	RES0603	DNP	Panasonic	ERJ-3GEYJ103V
17	1	TP71	WHITE	TH_TP_60D40	DNP	Keystone	5002
18	1	TP72	SMT	tp-smd40	DNP	NA	NA

NOTES:



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Tel: 86-23-8980-9588

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Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

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India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880-3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
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Fax: 43-7242-2244-393

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Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
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Fax: 33-1-69-30-90-79

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Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820